Model Requirements Rev. 13

Date: **February 2025**
Prepared By: **Electranix Corporation**

This document includes the following attachments:
Attachment #1: PSCAD Model Test Checklist for Reviewing Model Submissions

Revision 13 Notes (Changes from rev. 12):

Entire document	Editorial changes and clarifications in tables, figures and test names
Attachment 2	Attachment 2: Supplier compliance checklist removed
Requirements C,D,E,K	Additional clarity/focus on DC bus and energy source modeling, thermal protections, PPC delays, and as-left setting verification and associated model or documentation checks.
Footnote 2	Additional clarity on average source model features.
Requirement Y	Additional requirement for 32 and 64 bit Intel compiled models
Test list	Additional test measuring reaction time, and to check whether PPC/inverter comm delays are included
Test list	Clarified “Pmax” should be both charging and discharging for BESS systems.
Test list	Minor adjustments and fixes to existing tests, including adding ROCOF to frequency step test, reducing magnitude of voltage step test, additional operating points, and reduction in duration for LL fault test.

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Introduction

Specific model requirements for a PSCAD study depend on the type of study being done. A study with a scope covering weak system interconnections, ride-through evaluation, Sub-Synchronous Control Interactions (SSCI), short term[1] event response, and fast control interaction with nearby devices (for example) would require a model which has the following characteristics. Some specialty studies may require other features. Refer to "Attachment #1: PSCAD Model Test Checklist for Reviewing Model Submissions, appended to this document, for additional information on how these requirements may applied.

Validation of models against recorded equipment behaviour and benchmarking against other models are important tools for assuring accuracy. This document does not address how this validation or benchmarking should be done, but it is recommended that inverter and plant level validation be done to the extent practical and possible.

Model Accuracy Features

For the model to be sufficiently accurate, it must:

A. *Represent the full detailed inner control loops of the power electronics.* The model cannot use the same approximations classically used in transient stability modeling, and must fully represent all fast inner controls, as implemented in the real equipment. Models which embed the actual hardware code into a PSCAD component are currently wide-spread, and this is the required type of model.[2,3]

B. *Represent all control features pertinent to the type of study being done.* Examples include external voltage controllers, customized PLLs, ride-through controllers, SSCI damping controllers and others. As in point A, actual hardware code is required to be used for most control and protection features.

C. *Represent plant level control.* Power Plant Control (PPC) representation must be included which represents the specific controllers used in the plant. Plant controllers must be represented in sufficient detail to accurately represent short term performance, including transitions into and out of ride-through modes, settable control parameters or options, and any other specific implementation details which may impact plant behaviour. Generic PPC representations are not acceptable unless the final PPC controls are designed to exactly match the generic PPC model. If multiple plants are controlled by a common controller, or if the plant controller is controlling

[1] Example analysis periods could be 2 to 10 seconds following fault inception. Some studies could require longer periods.

[2] The model may be a full power transistor (eg. IGBT) representation, or use an average source representation that approximates the switching but maintains full detail in the inner controls, maintains DC side representation and protection features, maintains numerical stability when disconnected, and correctly mimics gate-blocking dynamics. Models manually translated block-by-block from MATLAB or control block diagrams may be unacceptable because the method used to model the electrical network and interface to the controls may not be accurate, or portions of the controls such as PLL circuits or protection circuits may be approximated or omitted. Note that firmware code should be directly used to create an extremely accurate PSCAD model of the controls. The controller source code may be compiled into DLLs or binaries if the source code is unavailable due to confidentiality restrictions.

[3] Model standards are under development which define appropriate ways to wrap .dll based control code into PSCAD models. Model writers are directed to "IEEE/Cigre Power System DLL Models/Standard" WG to assist in developing a DLL standard for controller models.

multiple types of resources (eg. Hybrid BESS/PV), this must be included in the plant control model. If supplementary or multiple voltage control devices (eg. STATCOM) are included in the plant, these should be coordinated with the PPC. All plant level communication delays should be included in the model, including transport delays, measurement delays, delays due to bus (eg. MODBUS) communication, sample and hold logic at the inverter or the PPC, and any other delay that may influence overall plant response in the time-frame of the study.

D. *Represent all pertinent electrical and mechanical configurations*. This includes any filters and specialized transformers (including grounding transformers). Mechanical features such as gearboxes, pitch controllers, PV panel dynamics, DC bus controllers, must be modelled if they impact electrical performance within the timeframe and electrical purview of the study. An infinite voltage source on the DC side is generally not acceptable. Battery resources must include the capability to represent the full range of state-of-charge levels. PV and wind resources must have capability to represent full range of active power availability. Any control or dynamic features of the actual equipment which may influence behaviour in the simulation period which are not represented or which are approximated must be clearly identified.

E. *Have all pertinent protections modeled in detail for both balanced and unbalanced fault conditions.* Typically this includes various OV and UV protections (individual phase and RMS), frequency protections, DC bus voltage/current protections, converter overcurrent protections, and often other inverter specific protections. Any protections which can influence dynamic behaviour or plant ride-through in the simulation period must be included. If there are mechanical limits which influence ride-through, such as thermal protection of wind turbine crowbar functions, these should be included in the model. Actual hardware code is recommended to be used for these protection features.

F. *Be configured to match expected site-specific equipment settings.* Any user-tunable parameters or options must be set in the model to match the equipment at the specific site being evaluated, as far as they are known. Default parameters are not appropriate unless these will match the configuration in the installed equipment.

Model Usability Features

In order to allow study engineers to perform system analysis using the model, the PSCAD model must:

G. *Have control or hardware options which are pertinent to the study accessible to the user.* Although plant must be configured to match site specific settings as far as they are known (see point F above), parameters pertinent to the study must be accessible for use by the model user. Examples of this could include protection thresholds, real power recovery ramp rates, frequency or voltage droop settings, voltage control response times, or SSCI damping controllers.[4] Diagnostic flags (eg. flags to show control mode changes or which protection has been activated) should be visible to aid in analysis.

[4] Care must be taken to ensure that any user-settable options are not changed in a way that is not implementable in the real hardware, and that any selectable options are actually available at the specific site being considered. Discussion is recommended with the manufacturer prior to any changes being made in model configuration.

H. *Be accurate when running at a simulation time step of 10 µs or higher*. Often, requiring a smaller time step means that the control implementation has not used the interpolation features of PSCAD, or is using inappropriate interfacing between the model and the larger network. Lack of interpolation support introduces inaccuracies into the model at larger simulation time-steps. In cases where the power transistor (eg. IGBT) switching frequency is so high that even interpolation does not allow accurate switching representation at 10 µs (eg. switching frequency greater than 40 kHz), an average source approximation of the inverter switching may be used to allow a larger simulation time step[2].

I. *Operate at a range of simulation time* steps. The model must not be restricted to operating at a single time step, but must be able to operate within a range (eg. 10 µs – 20 µs)

J. *Include documentation and a sample implementation test case.* Test case models must be configured according to the site-specific real equipment configuration up to the Point of Interconnection. This would include (for example): aggregated generator model, aggregated generator transformer, equivalent collector branch, main plant transformers, gen tie line, power plant controller, and any other static or dynamic reactive resources. Test case must use a single machine infinite bus representation of the system, configured with an appropriate representative SCR[5]. Access to technical support engineers is desirable. Additional detail on required documentation and test case is described in PSCAD Model Test Checklist (Appendix A).

K. *Have an identification mechanism for configuration.* The model documentation must provide a clear way to identify the specific settings and equipment configuration which will be used in any study, and tie these model parameters to as-left hardware settings at commissioning. This may be control revision codes, settings files, or a combination of these and other identification measures.

L. *Accept external reference variables.* This includes real and reactive power ordered values for Q control modes, or voltage reference values for voltage control modes. Model must accept these reference variables for initialization, and be capable of changing these reference variables mid-simulation, ie. dynamic signal references.

M. *Be capable of initializing itself.* Once provided with initial condition variables, the model must initialize and ramp to the ordered output without external input from simulation engineers. Any slower control functions which are included (such as switched shunt controllers or power plant controllers) must also accept initial condition variables if required. Note that during the first few seconds of simulation (eg. 0-2 seconds), the system voltage and corresponding terminal conditions may deviate from nominal values due to other system devices initializing, and the model must be able to tolerate these deviations or provide a variable initialization time.

N. *Have the ability to scale plant capacity.* The active power capacity of the model must be scalable in some way, either internally or through an external scaling component. This is distinct from a dispatchable power order, and is used for modeling different capacities of plant or breaking a lumped equivalent plant into smaller composite models.

[5] Representative SCR should reflect approximate N-1 interconnection SCR where possible, especially if the system is expected to be weak. If the system strength is not known, using a relatively low SCR in the test system, such as 2.5, may help to avoid issues during study phases.

O. *Have the ability to dispatch its output to values less than nameplate.* This is distinct from scaling a plant from one unit to more than one, and is used for testing plant behaviour at various operating points.

P. *Initialize quickly.* Model must reach its ordered initial conditions as quickly as possible (for example <5 seconds) to user supplied terminal conditions.

Study Efficiency Features

The following elements are required to improve study efficiency, model compatibility, and enable other studies which include the model to be run as efficiently as possible. These features represent best practices, and if any of these features are not supported, additional discussion is required[6]:

Q. Model must be compatible with Intel Fortran compiler versions 15 and higher.[7]

R. Model must be compatible with PSCAD version 5.0.2 and higher.

S. Model must support multiple instances of its own definition in the same simulation case.

T. Model must support the PSCAD "timed snapshot" feature accessible through project settings.

U. Model must support the PSCAD "multiple run" feature.

V. Model must not use or rely upon global variables in the PSCAD environment.

W. Model must not utilize multiple layers in the PSCAD environment, including 'disabled' layers.

X. Model must be compiled with Visual Studio 2015 or newer[8]

Y. Model should be supplied with both 32 bit and 64 bit compiled versions.[9]

[6] Electranix has parallelization tools available (E-Tran Plus for PSCAD) which can circumvent compatibility concerns in some cases.

[7] Models compiled using PSCAD with Intel Fortran 12 or 14 will use Visual Studio 2010 or 2013 which may cause compiler conflicts when those models are used in combination with models built with Intel Fortran 15 and newer. If Intel Fortran 12 or 14 support is required, it is recommended to compile both an Intel Fortran 12 to 14 model and an Intel Fortran 15 and newer model for maximum compatibility.

[8] Older models which were compiled using Intel Fortran 12 may not be compatible with Visual Studio versions 2015 or newer. In this case older versions of Visual Studio may be needed.

[9] Intel Fortran has discontinued support for 32 bit compilation going forward, but older compilers are still available and in use.

Attachment #1: PSCAD Model Test Checklist for Reviewing Model Submissions

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Purpose

This document is a test checklist meant to accompany "Model Requirements Rev. 13" (PMR) provided above. The checklist is intended for use by engineers who are reviewing model submissions, and the procedures provided in this document are intended to provide an indication of the plant model's accuracy, performance, and usability features as specified in the model requirements. These procedures cannot ultimately prove that the model is compliant with all requirements, as black box models usually hide the details of the equipment controls and protection. It is recommended that the equipment manufacturer supply additional confirmation that the model meets each individual requirement.

The tests outlined here are considered "minimal", and may be adjusted or supplemented by more rigorous testing to meet regional standards, as well as more extensive protection testing, benchmarking against phasor models, and validation against equipment measurement. The tests are subject to revision as the state of the art in EMT modeling evolves.

Model test Summary	
Model Test date:	
Reviewer	
Project Name:	
Interconnection Location:	
Rated Capacity at POI:	
Manufacturer:	
Equipment type: (eg. PV, Wind, BESS or Hybrid)	
Equipment version:	
Documentation files (OEM):	
Documentation files (site specific):	
Model Files supplied:	

Model Review Procedure and Checklist

		Yes/No	Comments
Documentation and site specific model verification			
1a	Model documentation states compliance with "Model Requirements Rev. Rev. 13" (PMR), including certification of model accuracy as defined in PMR.		
1b	The Vendor's name and the specific version of the model must be clearly observable in the. pscx PSCAD case.		
1c	OEM Documentation and supporting model filenames must not conflict with model version shown in the. pscx/.pslx file.		
1d	Documentation for how to use the plant model, including: - key parameters and any required information for configuring the model for the site matches supplied plant model. - Recommended range of simulation timesteps - Clear description of trip / operation code signals produced by model. - Description of how to check model parameters against "as left" settings.		
1e	Model is supplied with a runnable test circuit which is configured for the site-specific application.[10]		
"Real Code" model verification (Note that verification of real code relies upon statement of compliance)			
2a	Controls are black-boxed, and no PSCAD master library control blocks are visible within control circuits.[11] Model is based on "real code", with firmware version matching the expected installed version.[12]		
Model usability verification			
3a	Model uses a timestep greater than or equal to 10 µs[13]		
3b	Model is not restricted to running at a single defined timestep.		

[10] The test circuit must model all relevant electrical components of the plant and contain a system equivalent. Parameters will be assumed to be site-specific, unless there are obvious indications otherwise, such as an incorrect grid base frequency.
[11] Black-boxing of controls to a high level does not guarantee that real-code is embedded into the model, however the visibility of PSCAD master-library control blocks in the inner control loops (PLL, inner current controllers, etc.) suggest that the model is generic in nature. Model documentation may contain information on use of real-code in the model.
[12] If models are not "real code" models, all aspects of the controller operation are required to be validated by utilizing a "hardware in loop" platform or other hardware test systems. Validations must include control responses to various types of faults, changes in power and voltage references, changes in system frequency, testing frequency response in sub and super-synchronous ranges, and testing of protection operation. Tests must also be performed under a variety of system strengths, including very weak systems. If model control structures are significantly different /simplified from real equipment control structures, validation should be performed with multiple sets of realistic model parameters. Other tests may also be required. The validation report is required along with any model updates that result from the more rigorous validation tests.
[13] Models with timesteps less than 10 µs may be acceptable in situations where a small timestep does not significantly increase the runtime of the total simulation

3c	Model compiles using Intel FORTRAN 15 and Visual studio 2015 requirements in PMR, including versions compiled using both 32 bit and 64 bit options.		
3d	Model allows multiple instances of itself to be run together in the same case[14]		
3e	Model is supplied in both 32 bit and 64 bit compiled versions		
Model electrical configuration verification and screening for reasonable data			
4a	Plant level electrical single line diagram (SLD) is included.		
4b	Generator step-up transformer(s) included, with impedance between 5 and 10% on generator base, and matches SLD.[15]		
4c	Lumped collector equivalent(s) included for Wind Plants, with total charging equal to between 0.5 and 5% of plant rating, and matches SLD.[15]		
4d	Substation transformer(s) included which: - Is rated appropriately for plant size - Has impedance between 6 and 12% on transformer base[15] - Includes site specific tap configuration - Includes correct vector group or winding configuration - Matches transformer described in plant SLD		
4e	Model can be scaled to represent any number of inverters/turbines, either using a scaling transformer or internal scaling.		
4f	All supplementary devices included in the plant (such as STATCOMs) include appropriate models.		
4g	Inverter model includes representation of DC bus and energy source, with adjustable power availability for PV / wind and adjustable SOC for batteries.		
Plant controller verification			
5a	Model includes a power plant controller (PPC) with sufficient detail as described in PMR.		
5b	PPC accepts an external active power setpoint.		
5c	PPC accepts a voltage/reactive power/power factor setpoint.		
5d	PPC has a mechanism to implement a settable voltage droop.		
5e	If supplementary voltage control devices (eg. STATCOM/DVAR, SVC, MSCs) are included in the plant, ensure that the voltage control of these devices is effectively coordinated with the PPC, with no potential for VAR looping or oscillations.		

[14] Depending on specific application and whether E-Tran Plus for PSCAD is allowed to be used to overcome the limitation, this requirement may be waived.

[15] Impedance range is not prescriptive, and is included only for checking that entered parameters fall into a reasonable range. Impedances outside this range are allowed if the design so dictates.

5f	Communication delay is modeled between PPC and inverters		
Basic performance verification[16]			
6a	Initialization Tests: Model meet the success criteria in tests outlined in Table 1		
6b	Balanced Fault Ride-through tests: Model meet the success criteria in tests outlined in Table 2		
6c	Unbalanced Fault Ride-through tests: Model meet the success criteria in tests outlined in Table 3		
6d	Over-Voltage Ride-through Tests: Model meet the success criteria in tests outlined in Table 4		
6e	Voltage Reference Step Change Tests: Model meet the success criteria in tests outlined in Table 5		
6f	Active Power Reference Step Change Tests: Model meet the success criteria in tests outlined in Table 6		
6g	Grid Frequency Response and Ride-Through Tests: Model meet the success criteria in tests outlined in Table 7		
6h	Grid Voltage Phase Angle Change Ride-Through Tests: Model meet the success criteria in tests outlined in Table 8		
Supplementary and Informational Tests			
7a	POI SCR Change Tests (informational): Model meet the success criteria in tests outlined in Table 9		
7b	Voltage Protection Inclusion Tests: Model meet the success criteria in tests outlined in Table 10		
7c	PPC/Inverter delay test: Model meets the success criteria in tests outlined in Table 11		

[16] Performance testing is recommended with a POI level SCR of 2.5 and X/R of 5 as this is a representative system condition seen during weak system studies. Testing may be performed at higher SCRs if the lowest interconnection POI system strength under outage conditions is known to be higher.

Performance Verification Tests

Note on test system: Unless otherwise indicated, tests should be performed using a single source network equivalent in a moderately weak grid (eg. SCR = 2.5), or if the interconnection location system strength is calculable and known, the actual expected SCR may be used. The plant must ultimately comply with applicable ride-through standards within the context of the actual system, normally determined in a more complete interconnection study.

Note on OLTC: Tests should be performed with plant operating in a reasonable nominal state prior to the test. If an OLTC is used, tap should be set to produce an appropriate powerflow condition prior to the test.

Table 1: Initialization Tests

Test #	Test Description				Success Criteria
	Test duration [s]	Test Type	Active Power	Reactive Power	
1-1	20	Flat Run	Pmax[17]	0	Reach steady state within 5s
1-2	20	Flat Run	Pmin	0	Reach steady state within 5s

Table 2: Balanced Fault Ride-through Tests

Test #	Test Description					Success Criteria
	Fault duration [s]	Fault type	Fault impedance Zf	Active Power	Reactive Power	
2-1	0.16	3PHG	Zf=0	Pmax[17]	0	Ride Through
2-2	0.16	3PHG	Zf=0	Pmax[17]	Qmin	Ride Through
2-3	0.16	3PHG	Zf=0	Pmax[17]	Qmax	Ride Through
2-4	2.50	3PHG	Zf=Zs	Pmax[17]	0	Ride Through
2-5	2.50	3PHG	Zf=Zs	Pmax[17]	Qmin	Ride Through
2-6	2.50	3PHG	Zf=Zs	Pmax[17]	Qmax	Ride Through

Table 3: Unbalanced Fault Ride-Through Tests

Test #	Test Description					Success Criteria
	Fault duration [s]	Fault type	Fault impedance Zf	Active Power	Reactive Power	
3-1	0.16	2PHG	Zf=0	Pmax[17]	0	Ride Through
3-2	0.16	2PHG	Zf=0	Pmax[17]	Qmin	Ride Through
3-3	0.16	2PHG	Zf=0	Pmax[17]	Qmax	Ride Through
3-4	0.16	1PHG	Zf=0	Pmax[17]	0	Ride Through
3-5	0.16	1PHG	Zf=0	Pmax[17]	Qmin	Ride Through
3-6	0.16	1PHG	Zf=0	Pmax[17]	Qmax	Ride Through

[17] For Battery (BESS) systems, "Pmax" should be applied at full discharge (positive Pmax) and full charge (negative Pmax).

3-7	0.16	2PH	Zf=0	Pmax[17]	0	Ride Through
3-8	0.16	2PH	Zf=0	Pmax[17]	Qmin	Ride Through
3-9	0.16	2PH	Zf=0	Pmax	Qmax	Ride Through

Table 4: Over-Voltage Ride-Through Tests

Test #	Test Description				Success Criteria
	Fault duration [s]	Grid Voltage at POI (use infinite source at POI)	Active Power	Reactive Power	
4-1	1	1.2 pu	Pmax[17]	0	Ride Through
4-2	1	1.2 pu	Pmax[17]	Qmin	Ride Through
4-3	1	1.2 pu	Pmax[17]	Qmax	Ride Through

Table 5: Voltage Reference Step Change Tests

Test #	Test Description			Success Criteria
	Event	Active Power at POI	Initial Approx. Reactive Power at POI	
5-1	Connection point voltage change as per Figure 1	Pmax[17]	0	Step Response < 10s[1] Step Response > 1s[1]
5-2	Connection point voltage change as per Figure 1	Pmin	0	

[1] *Step response time measured at weakest known condition, or SCR = 2.5 if unknown. Step response time may be longer if agreed by connection utility.*

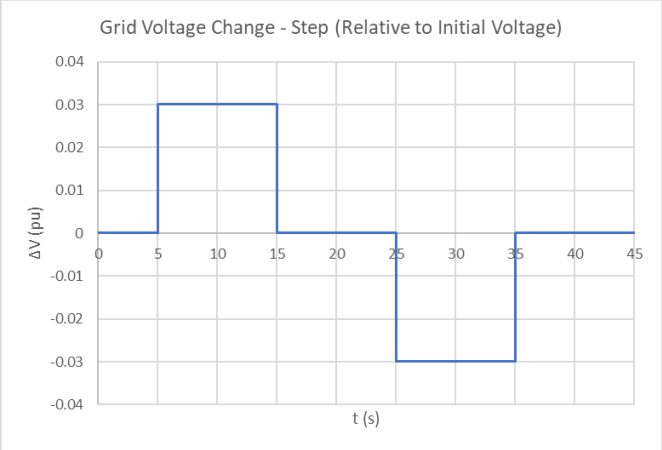

Figure 1: System voltage change

Table 6: Active Power Reference Step Change Tests

Test #	Test Description			Success Criteria
	Event	Active Power at POI	Initial Approx. Reactive Power at POI	
6-1	Active Power controller reference change as per Figure 2	Pmax	0	Plant Responds Appropriately

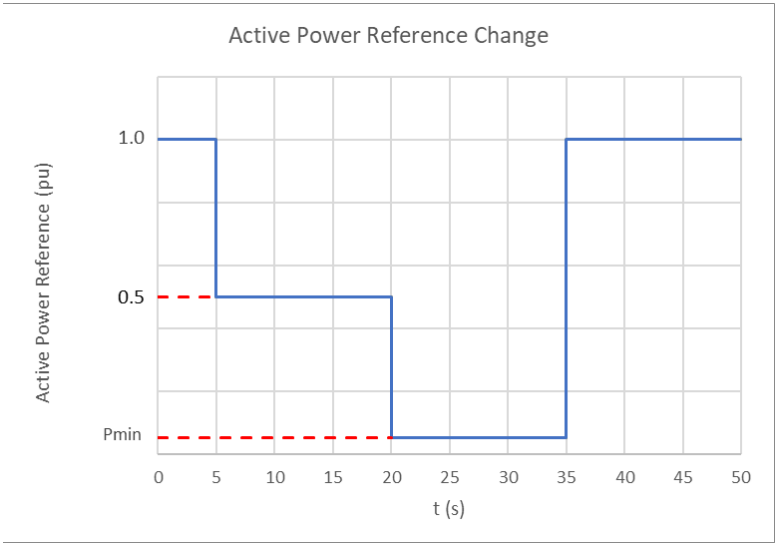

Figure 2: Active power reference step change

Table 7: Grid Frequency Response and Ride-through Tests

Test #	Test Description			Success Criteria
	Event	Active Power at POI	Initial Approx. Reactive Power at POI	
7-1	Grid Frequency Change as per Figure 3	Pmax[17]	0	Ride-through, Appropriate response per IEEE 2800 Tables7, Table 8, Figure 7 and table 15
7-2	Grid Frequency Change as per Figure 3	Pmin	0	
7-3	Grid Frequency Change as per Figure 4	Pmax[17]	0	
7-4	Grid Frequency Change as per Figure 4	Pmin	0	

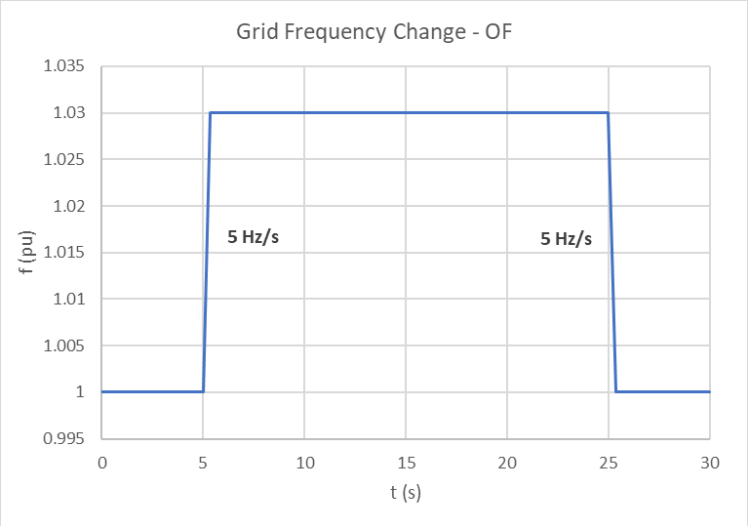

Figure 3: Grid frequency change (over-frequency)

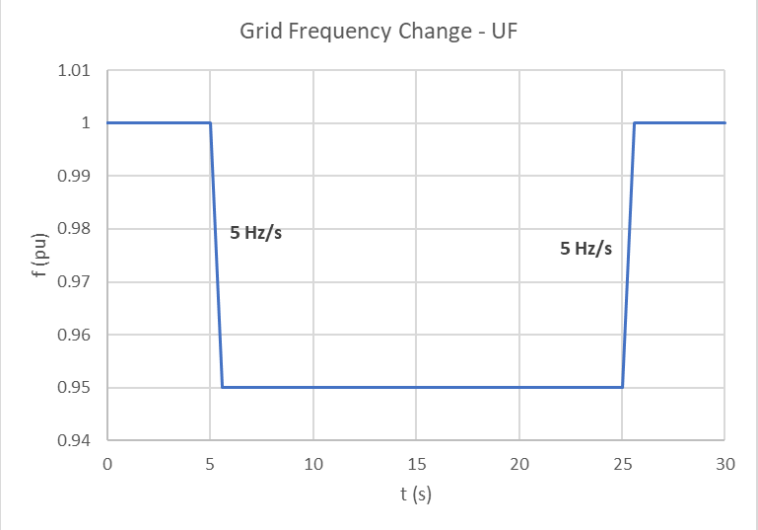

Figure 4: Grid frequency change (under-frequency)

Table 8: Grid Voltage Phase Angle Change Ride-through Tests

Test #	Test Description			Success Criteria
	Event	Active Power at POI	Initial Approx. Reactive Power at POI	
8-1	Grid voltage angle change equal to +25°	Pmax[17]	0	Ride Through
8-2	Grid voltage angle change equal to -25°	Pmax[17]	0	Ride Through
8-3	Grid voltage angle change equal to +25°	Pmin	0	Ride Through
8-4	Grid voltage angle change equal to -25°	Pmin	0	Ride Through

Supplementary and Informational Tests

Table 9: POI SCR Change Informational Tests[18]

Test #	Test Description			Success Criteria
	Event	Active Power at POI	Initial Approx. Reactive Power at POI	
9-1	Short Circuit Ratio (SCR) of the plant at POI is changed as per Figure 5. Before each SCR transition, a temporary (6 cycle) 3LG Z=0 fault is applied. SCR is changed during the fault, but prior to fault clearance. Time between transitions may be extended to allow stabilization. Note that the POI voltage and reactive current injection should be approximately maintained throughout the test.	Pmax[17]	0	For informational purposes only (not pass/fail) Plant is unlikely to show stable operation as SCR approaches 1.0[19]

[1] lower limit of stable behaviour may be lower with GFM converters

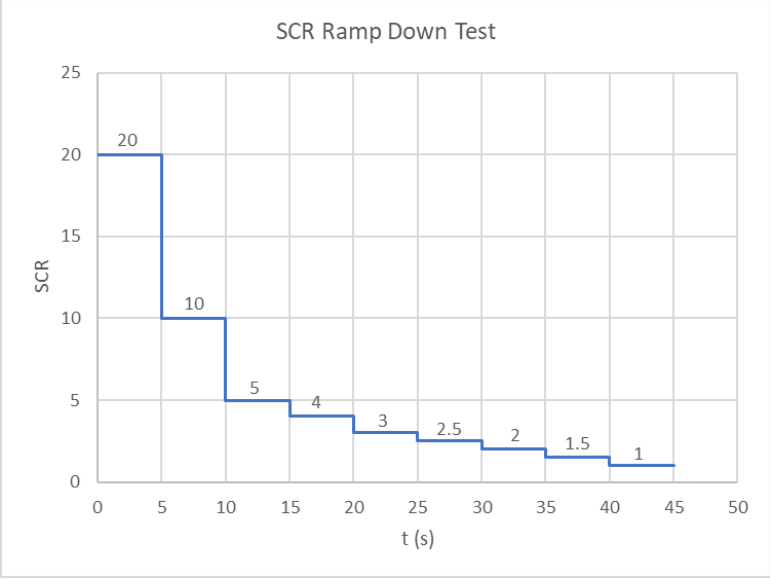

Figure 5: POI SCR change

[18] The purpose of this test not to pass or fail a converter, regardless of the results, but to understand both the stability limits of the plant as configured, and to understand the way that instability occurs. Different configurations or parameterizations may result in different results.

[19] Lower limit of stable behaviour may be lower with GFM converters

Table 10: Plant Response Time test

Test #	Test Description			Success Criteria
	Event	Active Power at POI	Initial Approx. Reactive Power at POI	
10-1	Connection point voltage change as per Figure 6	Pmax	0	Plant begins to respond between 100 ms and 200 ms following change in system voltage[20].

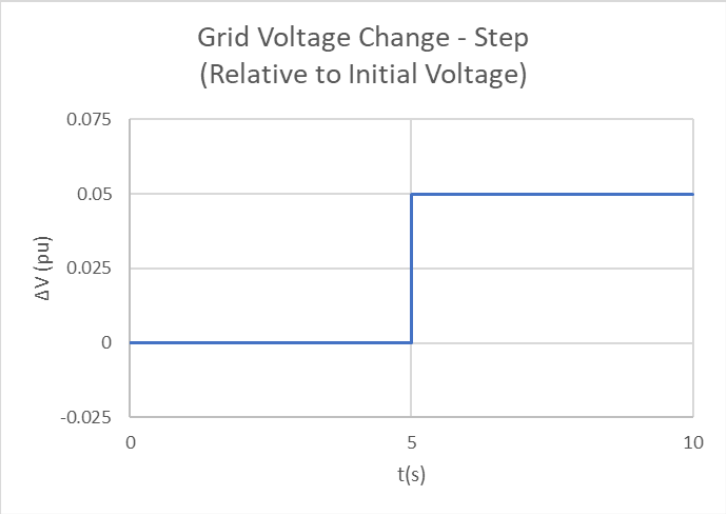

Figure 6: System voltage change

[20]Response (Reaction) should begin in less than 200 ms unless allowed to be longer by regional standards. Many models have not included delays caused by measurement, communication, data buses, or sample-and-hold, so reaction times less than 100 ms should be confirmed to be accurate

Table 11: Voltage Protection Inclusion Tests (Note that these tests only indicate that the model has protection included, and may vary according to equipment capability)

Test #	Test Description			Success Criteria
	Event	Active Power at POI	Initial Approx. Reactive Power at POI	
11-1	Grid Voltage step as per Figure 7	Pmax	0	Inverter Trips
11-2	Grid Voltage step as per Figure 8	Pmax	0	Inverter Trips

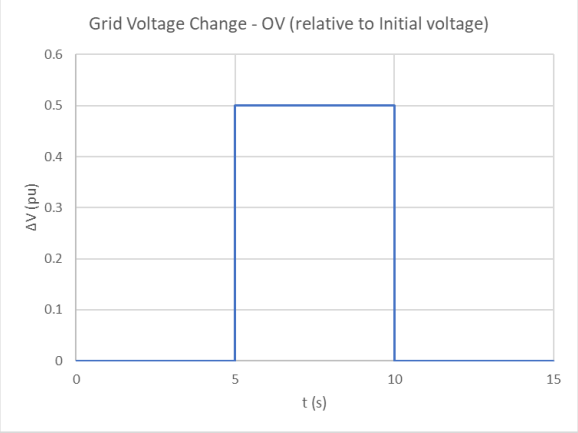

Figure 7: Grid voltage change - OV

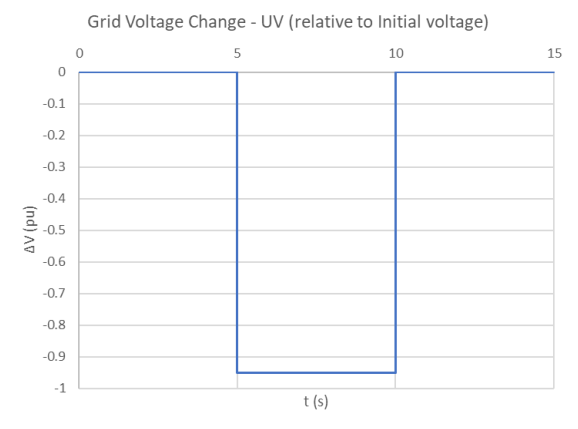

Figure 8: Grid voltage change - UV